ABSTRACT:

A method, system and computer program product for manipulating an instruction flow in a pipeline of a processor is disclosed. Detection means (142) detects an instruction of an instruction type that will lead to an interruption of the instruction flow through the pipeline. This is done by analyzing a relevant part of the instruction opcode, said opcode either representing a single instruction (400) or a plurality of instructions like a Very Long Instruction Word (420). Detection means (142) signals insertion means (180), which will flush redundant instructions from the pipeline, followed by the insertion directly into an intermediate pipeline stage (126) of an instruction that will aid the required switching of tasks. Aforementioned instruction opcode with recognizable bit pattern can be integrated in a computer program product, enabling optimized execution of the product by said system.

Figure 1